Sistemi multifunzionali integrati (Integrated multifunctional systems)

Table 3.18: Optimization based on variations of the thermal control law: problem statement (1).

Variables			
Name	**Min. value**	**Max. value**	**Description**
CONTRACT	1	4	Control law selector. Can only assume integer values (#).
HTRLAYOUT	1	2	Heater layout selector. Can only assume integer values (#).
QHMAX	2	12	Maximum power allowable for one heater. Real value (W).
TEMINIS	265	275	ON÷OFF law center temperature. Real value (K).
TLIM	250	270	Proportional law limit temperature. Real value (K).
TTH	270	290	Proportional law threshold temperature. Real value (K).
TSP	275	280	PID controller reference temperature. Real value (K).
TRISE	275	280	PTC heater switching temperature. Real value (K).

Table 3.19: Optimization based on variations of the thermal control law: problem statement (2).

Constraints		
Name	**Bounds**	**Description**
CONVIO1	<0	If positive, quantifies the extent of temperature range violation for electronics on the left side.
CONVIO2	<0	If positive, quantifies the extent of temperature range violation for electronics on the right side.
Objectives		
Name	**Direction**	**Description**
ENE	minimize	Energy required to feed the heaters during the whole simulation. Measured in kWh.
UNIFTEMP	minimize	Index for in-plane temperature evenness. Dimensionless quantity.

Table 3.20: Comparison of the optimal solutions in the first and second optimization studies.

Total energy (kWh)					**Temperature uniformity (#)**				
Proportional		**PID**	**Comparison**		**Proportional**		**PID**	**Comparison**	
			Absolute	Percentage				Absolute	Percentage
NCGA:	0.0348	0.0303	-0.0045	-12.93%	NCGA:	1.55	2.21	+0.66	+42.58%
Evol:	0.0423		-0.0120	-28.37%	Evol:	1.40		+0.81	+57.86%

data generated by the NCGA algorithm, while the second row refers to the Evol algorithm. The columns labeled as "PID" report the results of the new optimum point obtained in the second optimization. The columns labeled as "Comparison" present the variations between the old and new values, both in absolute (on the left) and percentage (on the right) terms. With respect to the figures in the actual ABB design, the new optimal solution characterized by layout n.2 and a PID control offers a 47% reduction in energy consumption, while the increase in the temperature uniformity index is now a small 9%. The best feasible points identified with the optimization study are all based on the PID logic, therefore these cases were isolated and the influence of the T_{sp} value on the global MFS performance was explored. It is clear that a positive correlation of this parameter exists both for the total energy consumption and for the unevenness of the in-plane temperature distribution (see Figures 3.29 and 3.30). The two clearly distinct sets that can be observed in Figure 3.30 are due to the two different layouts. In these pictures, black dots represent feasible solutions, while grey dots are feasible solutions which extremize one of the objective functions. The only white dot is the overall optimal solution. Regarding Figure 3.29, the horizontal axis shows the set point temperature (measured in Kelvin), while the vertical axis shows the total energy consumption (measured in kWh). As concerns Figure 3.30, the horizontal axis shows the set point temperature (measured in Kelvin), while the vertical axis shows the temperature uniformity index (dimensionless quantity).

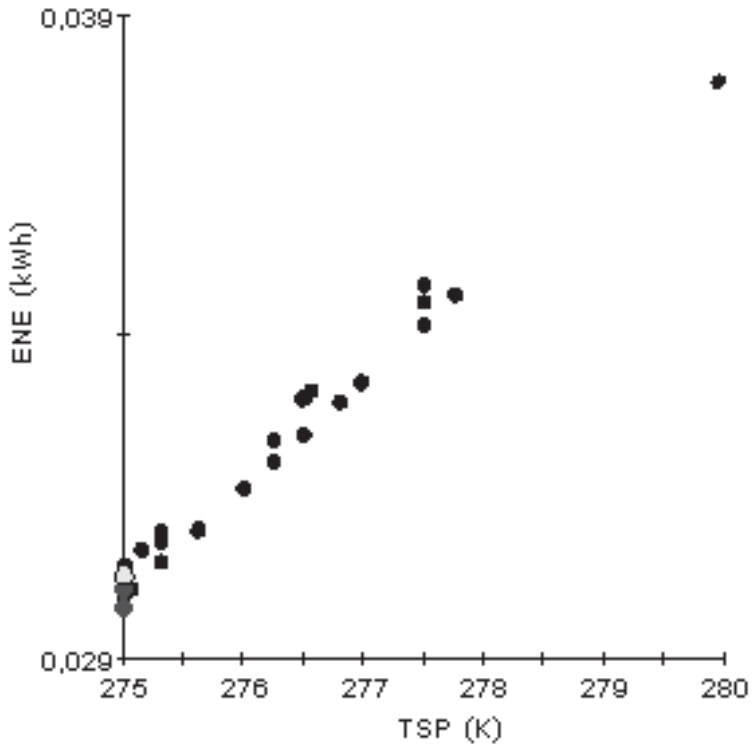

Figure 3.29: Total energy consumption vs. set point temperature of the PID controller.

The results obtained from the optimization process confirm that, if it is not possible to embed a predictive description of the system to be controlled in the

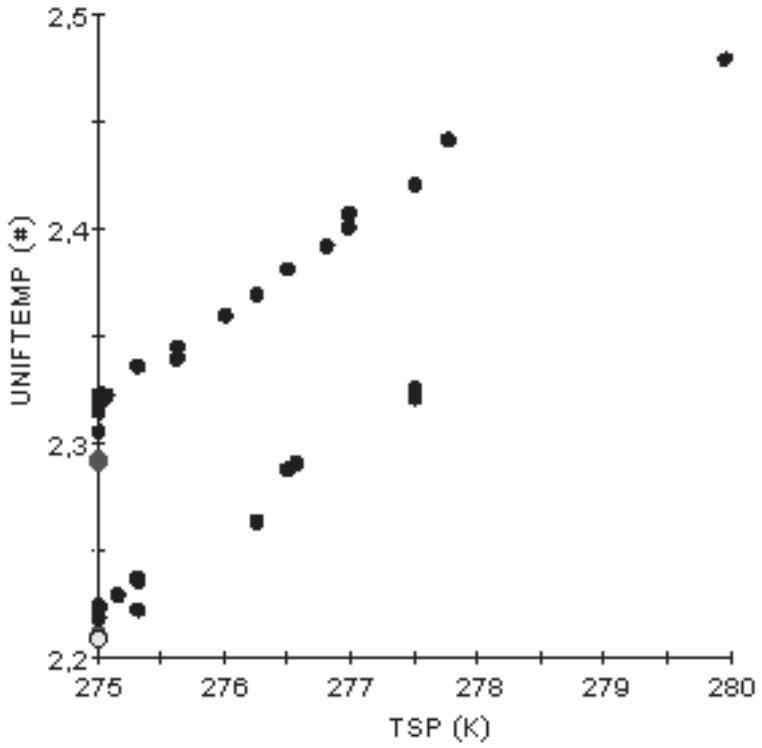

Figure 3.30: Temperature uniformity index vs. set point temperature of the PID controller.

controller, a PID logic is surely a good choice. Like many other feedback logics, it will solely rely on a reactive mechanism, but the performance will be much better. Unfortunately, PID strategies are best employed in linear symmetric problems, in which the variable to be controlled can be corrected both with positive and negative commands: in the present case, since there is no active cooling piloted by the PID, is it only possible to affect the variables with positive commands (increasing temperature), while overshoots can only be minimized with an over-damped configuration, but cannot be actively corrected. Nonetheless, it is interesting to investigate the possibility obtaining further benefits from the PID controller through a better tuning of its parameters: this has been the content of an additional optimization study.

Focus was therefore concentrated on the best configuration, in an attempt to obtain further improvements. To this aim, a third optimization study, which is summarized in Tables 3.21 and 3.22, was performed. This time only the Proportional-Integral-Derivative logic was adopted, and its six parameters (the heater layout, the maximum power fed to one heater, the PID set point temperature and the three PID constants) were left free for possible changes.

The problem has been solved with a Neighborhood Cultivation Genetic Algorithm (NCGA), based on a population size of 20, a number of generations equal to 50, single point crossover with a crossover rate equal to 1.0, and a mutation rate equal to 0.01. The NCGA run lasted 17.27 hours and produced 959 feasible designs from over 1001 evaluations. The genetic algorithm identified a Pareto set

Table 3.21: Optimization based on variations of the thermal control law: problem statement (1).

Variables			
Name	**Min. value**	**Max. value**	**Description**
HTRLAYOUT	1	2	Heater layout selector. Can only assume integer values (#).
QHMAX	5	7	Maximum power allowable for one heater. Real value (W).
TSP	272	275	PID controller reference temperature. Real value (K).
KPPID	-8.4	-6	PID controller proportional gain. Real value (W K^{-1}).
KIPID	-67	-47	PID controller integral gain. Real value (W K^{-1} s^{-1}).
KDPID	-0.08	-0.03	PID controller derivative gain. Real value (W s K^{-1}).

Table 3.22: Optimization based on variations of the thermal control law: problem statement (2).

Constraints		
Name	**Bounds**	**Description**
CONVIO1	<0	If positive, quantifies the extent of temperature range violation for electronics on the left side.
CONVIO2	<0	If positive, quantifies the extent of temperature range violation for electronics on the right side.
Objectives		
Name	**Direction**	**Description**
ENE	minimize	Energy required to feed the heaters during the whole simulation. Measured in kWh.
UNIFTEMP	minimize	Index for in-plane temperature evenness. Dimensionless quantity.

of solutions. The solution characterized by the values reported in Table 3.23 was selected. Its energy consumption was 0.0278 kWh, while the temperature evenness index was 2.16.

This results, in comparison with the PID solution of the previous optimization, reduced the energy consumption by another 8%, while the enhancement of the isothermal condition of the panel was only about 2%. The small improvement obtained, in terms of temperature uniformity, confirms that this figure of merit mainly depends on the heater distribution, rather than on the thermal control law. Table 3.24 summarizes the benefits obtained with the optimization of the PID parameters. The columns labeled "Previous optimum" summarize the results of the old optimum points, i.e. the optimal solutions presented in the first and second optimization runs. The first row contains data generated by the NCGA algorithm in the first study, the second row refers to the Evol algorithm in the first study, and the third row includes the solution obtained in the second study. The columns labeled "New optimum" report the results of the new optimum point obtained in this third study via NCGA. The columns labeled "Comparison" present the variations between the previous and new optima, both in absolute (on the left) and percentage (on the right) terms. In comparison with ABB, the new design allows a 52% reduction in energy consumption, and limits the increase in temperature uniformity index to 7%.

From the energy saving point of view, it could be possible to obtain some further small improvements (about one percentage point, that is < 1 Wh) by selecting heater layout number 1, but at the same time this choice would deteriorate the *UNIFTEMP* index. Since the enhancement of the energy budget would be minimal, it would be better to choose the solution that allows a smoother temperature distribution on the upper skin.

The presence of a feasible solution with lower energy expenditure can be noticed in Figure 3.31. In this picture, the light grey dot is a feasible solution which minimizes the temperature uniformity index. Black dots (upper right quadrant) are feasible solutions, while dark grey dots (bottom left quadrant) are unfeasible solutions (with non-zero constraint violation). The only white dot is the overall optimal solution, and grey lines are just visual aids to locate the optimum and read the value of its parameters on the two axes. The horizontal axis shows the set point temperature, measured in Kelvin, while the vertical axis shows the total energy consumption, measured in kWh. A second genetic algorithm based optimization was carried out with AMGA (Archive-based Micro Genetic Algorithm) with an initial size of 80, a population size of 80, a number of function evaluations equal to 1000, a crossover probability equal to 0.9, and a mutation probability equal to 0.5. The computation lasted 17.18 hours. This second search identified an optimal solution that is very similar to the previous one: a maximum required energy of 0.0277 kWh, and a temperature uniformity index of 2.16. Therefore, the advantages obtained compared to an ON÷OFF or proportional rule are almost identical to those shown in Table 3.24. This fact confirms the reliability of the previously identified optimum point. The PID parameters of this solution are summarized in Table 3.25.

As a final check, the stability of the best control law was verified via a dedicated simulation. The results confirmed that the temperature behavior was totally free of

Table 3.23: PID controller parameters in the NCGA optimum solution.

HTRLAYOUT	**QHMAX (W)**	**TSP (K)**	**KPPID (W K^{-1})**	**KIPID (W K^{-1} s^{-1})**	**KDPID (W s K^{-1})**
2	5.82	273.45	-6.72	-47.07	-0.06

Table 3.24: Comparison of the new optimum solution (third study) with the optimal results of first and second optimization study.

Total energy (kWh)					**Temperature uniformity (#)**				
Previous optimum		**New optimum**	**Comparison**		**Previous optimum**		**New optimum**	**Comparison**	
			Abs.	Perc.				Abs.	Perc.
NCGA Proportional (first study)	0.0348	0.0278	-0.0070	-20.12%	NCGA Proportional (first study)	1.55	2.16	+0.61	+39.36%
Evol Proportional (first study)	0.0423		-0.0145	-34.28%	Evol Proportional (first study)	1.40		+0.76	+54.29%
NCGA PID (second study)	0.0303		-0.0025	-8.28%	NCGA PID (second study)	2.21		-0.05	-2.26%

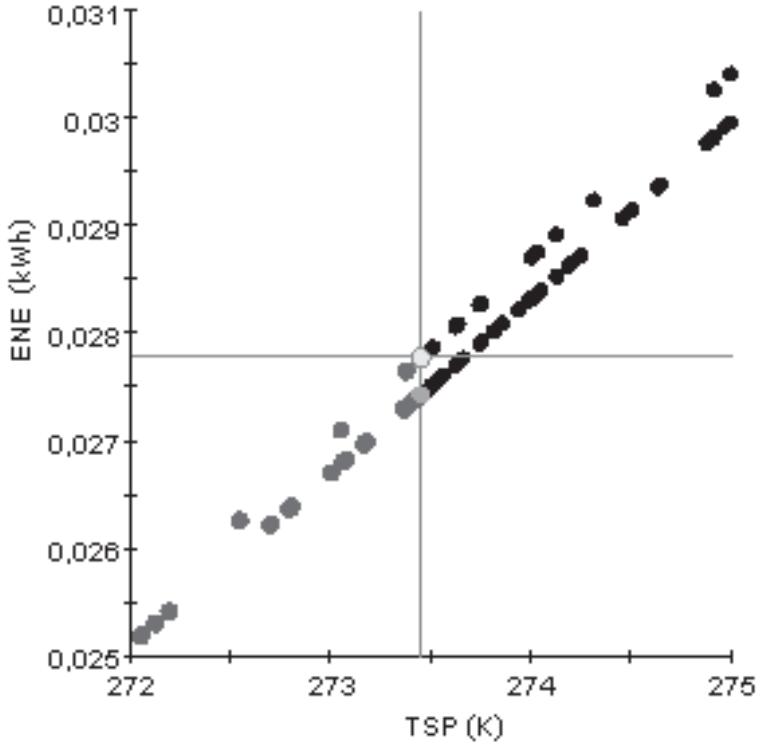

Figure 3.31: Total energy expenditure vs. set-point temperature of the PID controller.

Table 3.25: PID controller parameters in the AMGA optimum solution.

Parameter	**value**
HTRLAYOUT	2
QHMAX (W)	5.19
TSP (K)	273.42
KPPID (W K^{-1})	-6.34
KIPID (W K^{-1} s^{-1})	-61.36
KDPID (W s K^{-1})	-0.05

undesired oscillations. In order to assess the robustness of the improvement obtained with the PID logic, white noise was injected upstream from the controller input in a dedicated dynamical model of the panel. This noise would roughly simulate a general EMI/EMC problem that affects, for example, the sensors. As a result, the system response obviously showed some oscillations in the regulated temperatures (of the order of $1 \div 2$ K), but the overall energy consumption did not change: only small negligible fluctuations were registered with a noise power - i.e. height of the noise PSD - of 0.01 or 0.1.

3.2 Testing

3.2.1 ABB testing

Thermal Vacuum Test generalities

The main purposes of the test were:

- To estimate the thermal performance of the panel in terms of heat rejection capability in different power dissipation configurations.
- To verify the behavior of COTS electronics in a thermal-vacuum environment representative of space applications.
- To verify mechanical and thermal behavior of flexible PI/Cu circuitry.

Test facility

The TV test was carried out in the Leybold Space Chamber, at Thales Alenia Space premises. The facility has an internal capacity of 650 liters, and the usable volume is enclosed in a horizontal axis cylinder of diameter 800 mm and length 1200 mm. The temperature range achievable by the shrouds is:

- -180 deg C, with LN2
- -50 to +80 deg C, with silicone oil circuit
- ambient temperature to +100 deg C, with heaters

and temperature accuracy is $\pm$ 1 deg C (in the range -50 to +80 deg C). The ultimate achievable pressure is $<$ 2E-5 mbar.

TVT set-up and instrumentation

Additional heat loads have been simulated by means of 5 electrical heaters, labeled as H1...H5 in Figure 3.35. Heater layout and nominal power are shown in Table 1. The five heaters have been activated all together and in combination with dummy electronics on the two motherboards. The possibility has been assured to switch on independently each resistor.

The test article has been instrumented with a suitable number of thermocouples:

Figure 3.32: Leybold Thermal Vacuum Chamber, outer view.

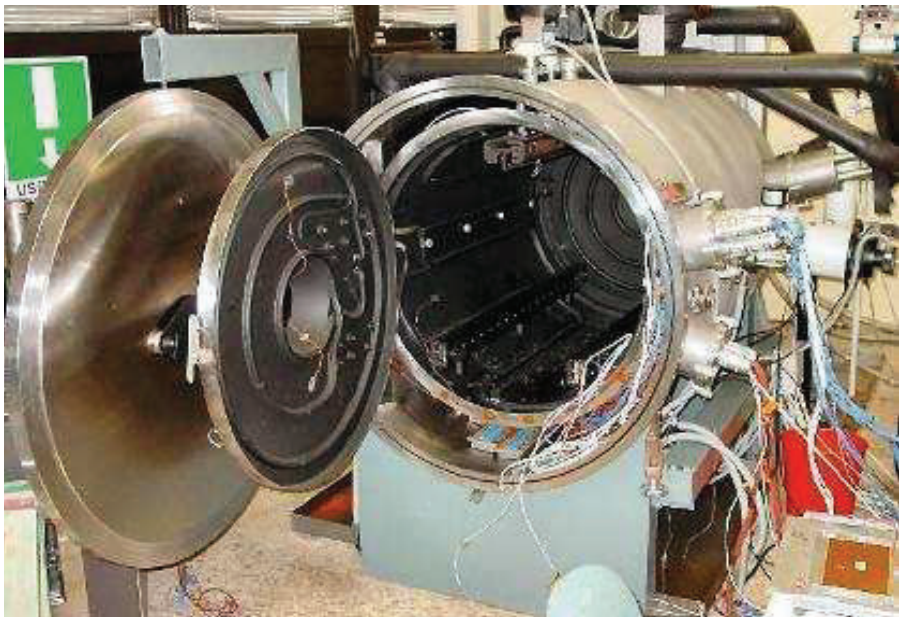

Figure 3.33: Leybold Thermal Vacuum Chamber, inner view.

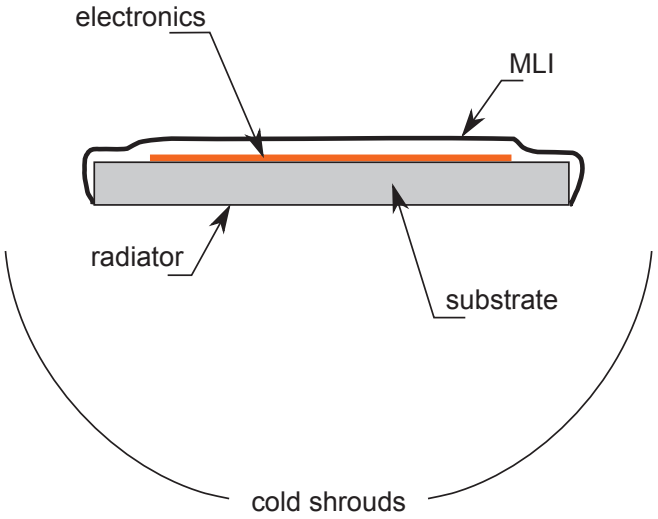

Figure 3.34: ABB Test set-up, sketch.

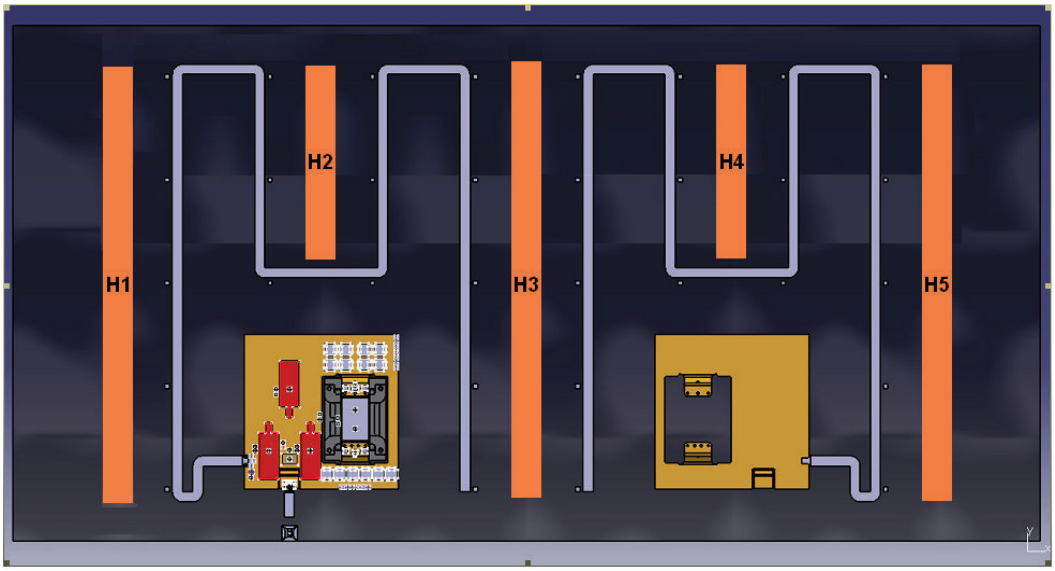

Figure 3.35: ABB Test set-up, sketch.

Table 3.26: ABB heater data.

Heater	Type	Resistance (Ω)	Max power (W)
H1	Clayborn 4 wires A28	5.88	230
H2	RICA double conductor	129.52 (257 a pista)	200
H3	Clayborn 4 wires A28	5.91	230
H4	RICA double conductor	131.86 (262 each)	200
H5	Clayborn 4 wires A28	6.26	230

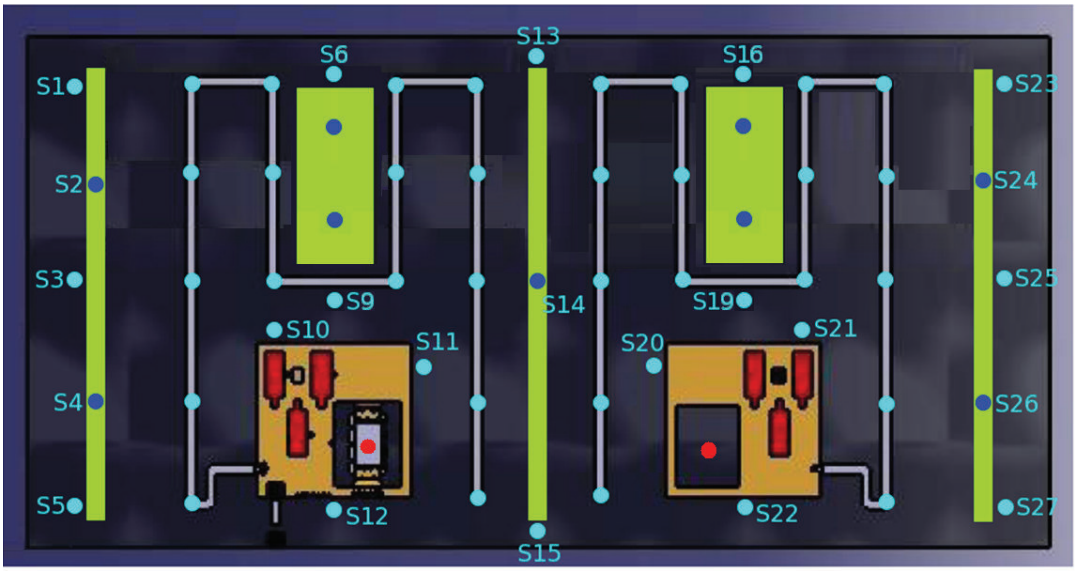

Figure 3.36: Layout of temperature sensors, +z skin. Blue circles are TCs on top of heaters. TCs on H2 and H4 are not labelled for lack of space. They are: $H2_{top} = S7$; $H2_{bottom} = S8$; $H4_{top} = S17$; $H4_{bottom} = S18$. Red circles are TCs on top of DC/DC converters, they are : $DC_{left} = S82$, $DC_{right} = S81$.

- Two TCs on the external side (i.e. facing the chamber) of the MLI blanket and two on the internal side.
- 29 TCs on the +z skin (cyan, blue and red circles in the sketch of Figure 3.36).
- 53 TCs on the -z skin (red crosses in the sketch of Figure 3.37).

Moreover, two networks made of 37 direct-to digital temperature sensors are linked to the two motherboards: these sensors represent additional instrumentation of the test article. Integrated thermal monitoring circuit can indeed be used to collect data, avoiding the connection of further TCs.

All bundles were insulated with 10 layers MLI and properly instrumented with TCs.

The +z skin of the test article has been properly insulated with 20-layers MLI blanket.

The electrical connections were led out of the thermal-vacuum chamber through use of special leakproof feedthroughs.

Additional equipment used to carry out the test was:

- One 110V DC power units (maximum power 1000W), in order to feed the DC/DC converters.
- Two PCs, in order to gather data from Dallas sensors.
- Two USB cables, in order to read USB ports (as mentioned in the ABB description, temperature data is converted from OneWire protocol to USB protocol and routed outside TVC via two miniB-to-standardA USB cables).

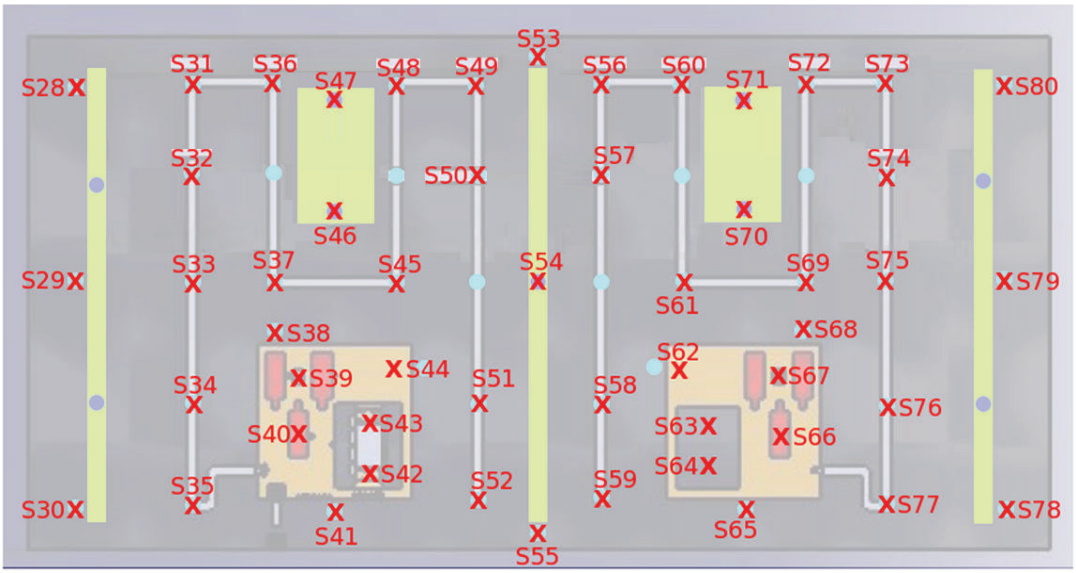

Figure 3.37: Layout of temperature sensors, -z skin.

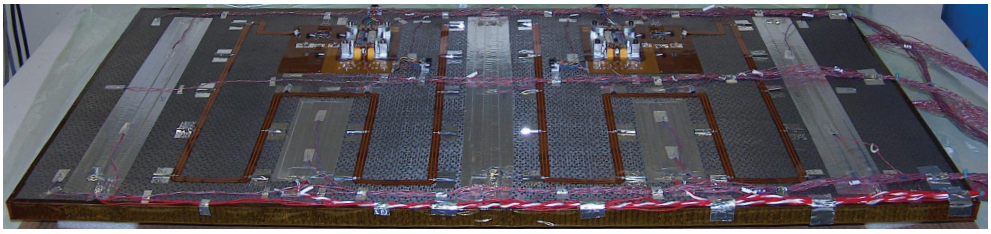

Figure 3.38: Upper face of the panel (+z skin) without MLI.

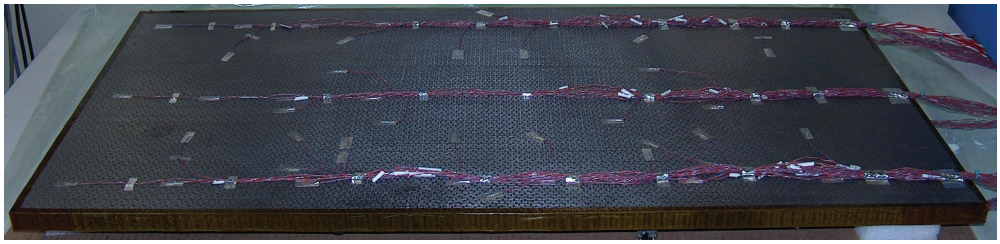

Figure 3.39: Lower face of the panel (-z skin).

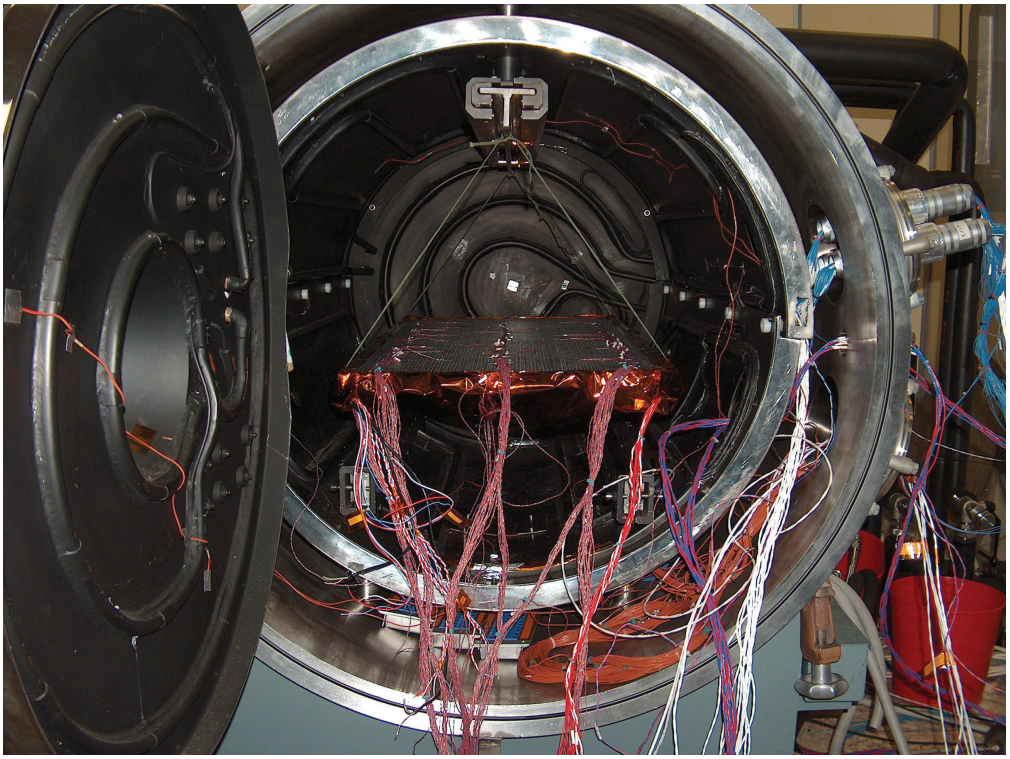

Figure 3.40: Test panel assembly while suspended into the thermal-vacuum test chamber.

Test approach

The test article has been suspended inside the Leybold vacuum chamber (Figure 3.40). The test consisted of a thermal balance test under simulated space environment conditions by thermally controlled shrouds. Test environment conditions were:

- Vacuum: $P < 10e - 5$ bar.
- shroud temperature: T = -180 °C.
- upper face (+z skin) of the panel (mounting electronics) isolated with 20-layers MLI blanket.
- lower face (-z skin) exposed to shrouds.

Temperature data from the integrated electronics and from auxiliary sensors have been acquired and saved for the whole duration of the test with a suitable scan rate ($\Delta t = 60\ s$ for thermocouples, $\Delta t = 10 \div 12\ s$ for Dallas sensors).

Various plateaus have been carried out, characterized by different power levels, according to the test sequence described in Table 3.28.

During test, scrupulous attention was paid to COTS electronics requirements, in particular, to limit temperatures. Consult Table 3.27 for details.

Table 3.27: Temperature limits for ABB electronics.

Component	**Description**	**Inoperative range**		**Operative Range**	
		T Min [°C]	T Max [°C]	T Min [°C]	T Max [°C]
Dallas DS9503	ESD Protection	-55	+125	-40	+85
Dallas DS2490	USB to 1Wire	-55	+125	0	+70
IQD CFPS-73	SMD clock oscillator	-55	+125	0	+70
MAXIM MAX8881	ultra-low supply curr.	-65	+165	-40	+85
VICOR MICRO V110C28M100BF	DC-DC converter	-65	+125	-55	+100
DS18B20U	Temperature Sensor	-55	+125	-55	+125
HK5582R5.3L12A	Minco Kapton Heater	-200	+200	-200	+200

Table 3.28: Test sequence for thermal vacuum test.

Step	Phase	Description	Details
1	Phase 1	Initial Checks	As needed
2		Start OneWire acquisition	
3		Pumpdown	Vacuum level: $P < 10e-5$ bar
4		Shroud cooling down to -180 °C	Motherboard heaters on to ensure limit inoperative temperature to electronics
5	Phase 2	H1, H3, H5 on at low power level	25 W
6		H2, H4 on at low power level	12.5 W
7		Heaters on MB left and MB right on	12.5 W
8		Temperature Stabilization	125 W total (*)
9		Stop LN2, start shroud heating	
10		Heaters on MBs off	
11		H1 to H5 off	When shrouds have reached minimum non operative temperature for electronics
12		Stop OneWire acquisition	
13		Shroud heating up to +20 °C	To avoid letting TVC shrouds cold during short test break
14	Phase 3	Start OneWire acquisition	
15		Shroud cooling down to -180 °C H1, H3, H5 on to ensure limit inoperative temperature to electronics	30 W
16		H1, H3, H5 on at medium power level	50 W
17		H2, H4 on at medium power level	20 W
18		Temperature Stabilization	190 W total (*)
19		Stop LN2, start shroud heating	
20		H2, H4 off	

Table 3.28: Test sequence for thermal vacuum test.

Step	Phase	Description	Details
21		H1, H3, H5 off	When shrouds have reached minimum non operative temperature for electronics
22		Stop OneWire acquisition	
23		Shroud heating up to +20 °C	To avoid letting TVC shrouds cold during short test break
24	Phase 4	Start OneWire acquisition	
25		Shroud cooling down to -180 °C H1 on to ensure limit inoperative temperature to electronics	50 W
26		H1 on at high power level	100 W
27		Temperature Stabilization	100 W total (*)
28		Stop LN2, start shroud heating	
29		H1 off	When shrouds have reached minimum non operative temperature for electronics
30		Stop OneWire acquisition	
31		Shroud heating up to +20 °C	To avoid letting TVC shrouds cold during short test break
32	Phase 5	Start OneWire acquisition	
33		Shroud cooling down to -180 °C H5 on to ensure limit inoperative temperature to electronics	100 W
34		H5 on at high power level	100 W
35		Temperature Stabilization	100 W total (*)
36		Stop LN2, start shroud heating	
37		H5 off	When shrouds have reached minimum non operative temperature for electronics
38		Stop OneWire acquisition	

Table 3.28: Test sequence for thermal vacuum test.

Step	Phase	Description	Details
39		Shroud heating up to +20 °C	To avoid letting TVC shrouds cold during short test break
40		Pressure Recovery (to ambient)	To avoid letting cryopump working during long test break
41	Phase 6	Start OneWire acquisition	
42		Pumpdown	Vacuum level: $P < 10e-5$
43		Shroud cooling down to -180 °C Right MB heaters and H1 on to ensure limit inoperative temperature to electronics	Right MB to 15 W H1 to 25 W
44		H1 on at medium power level	50 W
45		Right MB heaters on at medium power level	30 W
46		Temperature Stabilization	80 W total (*)
47		Stop LN2, start shroud heating	
48		MB heaters off	
49		H1 off	When shrouds have reached minimum non operative temperature for electronics
50		Stop OneWire acquisition	
51		Shroud heating up to +20 °C	To avoid letting TVC shrouds cold during short test break
52	Phase 8	Shroud cooling off	
53		Pressure Recovery (to ambient)	
54		Power switch off	
55		Final Checks	

(*) Stabilization criterion: $\Delta T < 0.5$ °C/hr, measured near the powered heaters.

3.2.2 STEPS Smart Skin testing

This test campaign is divided in two batches: a thermal vacuum test and an ambient thermal test.

The thermal vacuum test plan included two breadboards:

- SDA, STEPS demonstrator A
- SDB, STEPS demonstrator B

The first breadboard consists of a rectangular aluminium honeycomb panel, equipped with four Smart Skin Motherboards, while the second breadboard consists of a curved aluminium shell hosting a single Smart Skin MB. These two prototypes are wired together to form a single communication network and tested during the same TVT.

The ambient test includes a single breadboard, SDC (STEPS demonstrator C), which consists of one Smart Skin MB glued on a Kevlar fabric patch. This demonstrator is tested at room conditions in the Thermal Control Technological Area.

From the validation test campaign, the following results are expected:

- successful validation of the bonding process (smart-skin to substrates).
- successful validation of COTS components in their operative conditions range.
- successful validation of the smart skin design in a representative thermal-vacuum environment.
- successful validation of the smart skin control software and user interface.
- critical investigation of possible design weaknesses and subsequent assessment of future improvements.

Thermal Vacuum Test generalities

The main purposes of the test are:

- To verify the behavior of COTS electronics in a thermal-vacuum environment representative of space applications.
- To verify mechanical and thermal behavior of flexible PI/Cu circuitry.

The thermal-vacuum test campaign is carried out in TAS-I Leybold facility, and for information regarding the chamber the reader can refer to the corresponding subsection of the ABB test description.

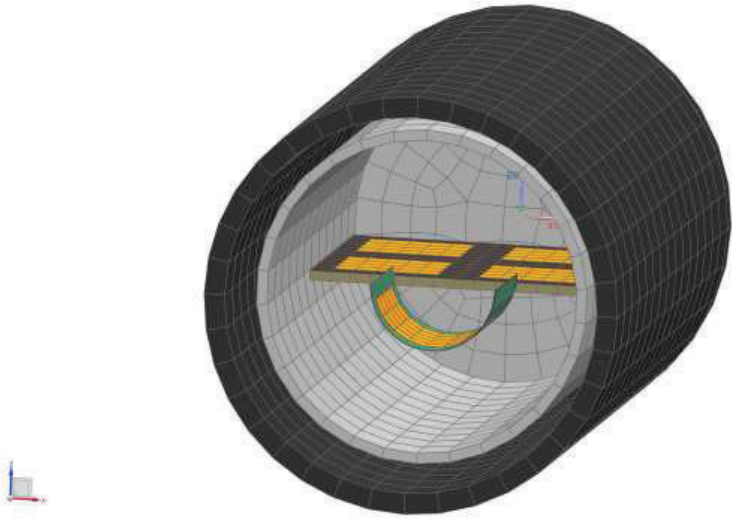

Figure 3.41: SDA and SDB panels inside the TVC.

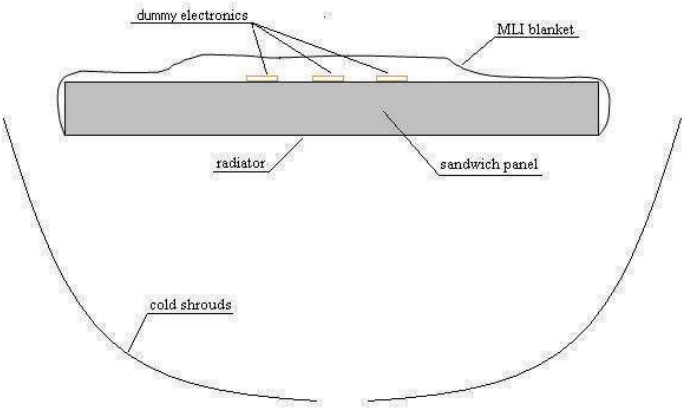

Figure 3.42: Test set-up, sketch.

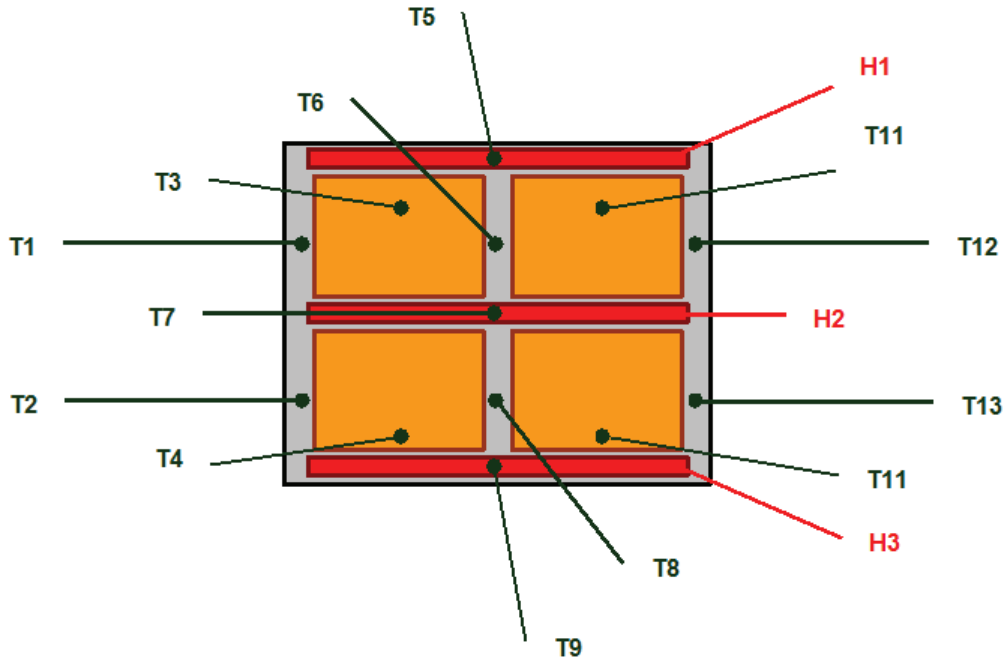

Figure 3.43: Heaters and thermocouples labeling (SDA, electronic side).

TVT set-up and instrumentation

Both SDA and SDB are suspended together inside the Leybold vacuum chamber, as depicted in Figure 3.41.

Each panel has the electronic side properly insulated with 20-layers MLI blankets (see Figure 3.42), while the other side directly faces the cold shrouds. In both demonstrators, all electronic items are insulated (with a polymeric foil) from the MLI inner metallic foil, in order to avoid short circuits on exposed pads.

Aboard the SDA panel, thermal loads are simulated by means of 3 electrical heaters, labeled as H1...H3 in Figure 3.43. Heater layout and nominal power are shown in Table 3.29. The 3 heaters, in parallel connection, can be activated all together, and in combination with dummy units on the four motherboards. The test article is instrumented with a suitable number of temperature sensors (thermocouples - TCs):

- 2 TCs on the external side (i.e. facing the chamber) of the MLI blanket and 2 on the internal side;
- 13 TCs on the demonstrator +z skin (electronic side);
- 13 TCs on the demonstrator -z skin (chamber side).

Figure 3.43 and Figure 3.44 show position and numbering of the 26 SDA thermocouples. Moreover, 4 sub-networks (made of 17 direct-to-digital temperature sensors each) are hosted on the four motherboards, for a grand total of 68 monitoring points: these sensors represent additional instrumentation of the SDA test article. Integrated thermal monitoring circuit can indeed be used to collect data, avoiding

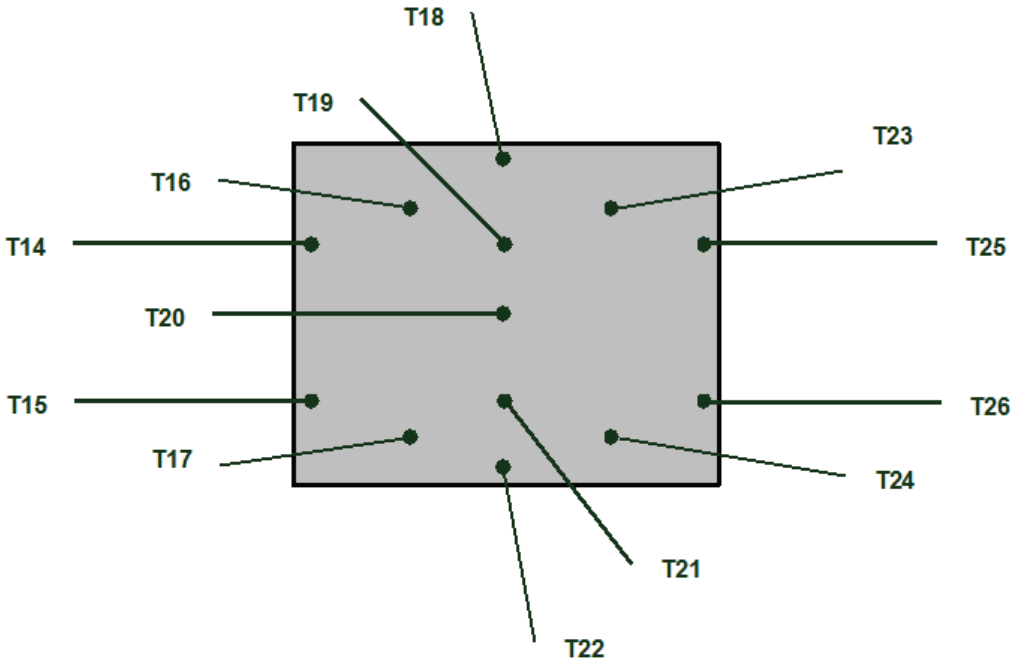

Figure 3.44: Layout of temperature sensors on -z skin (SDA, chamber side).

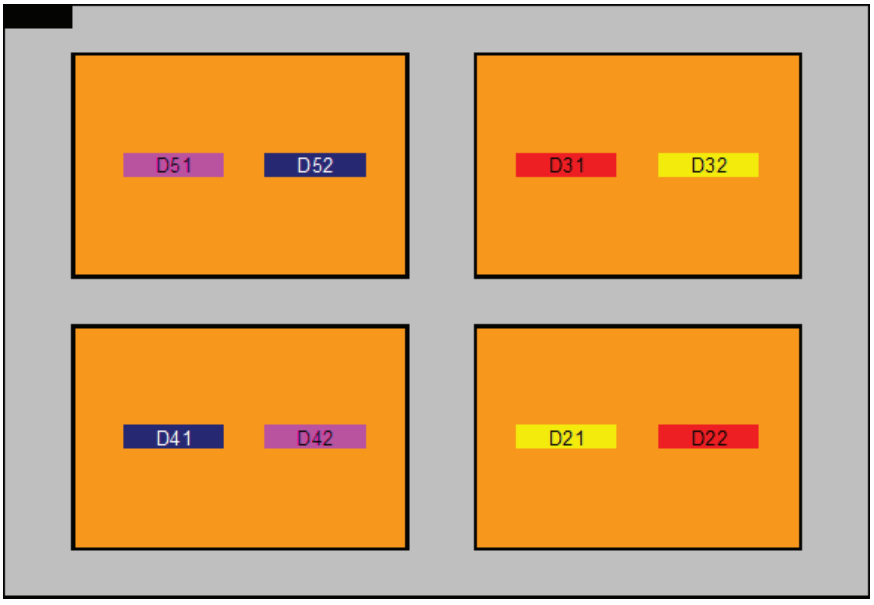

Figure 3.45: Dummy units onboard SDA (same color means that they are connected to the same power supply). Black corner is axes origin.

Table 3.29: SDA heater data.

Heater	**Type**	**Length (mm)**	**Resistance (Ω)**	**Max power (W)**
H1	Clayborn (A28, 4 wires, 70 W/ft)	∼ 640	∼16 (15.15)	>100 (∼147)
H2	Clayborn (A28, 4 wires, 70 W/ft)	∼ 640	∼16 (15.26)	>100 (∼147)
H3	Clayborn (A28, 4 wires, 70 W/ft)	∼ 640	∼16 (15.15)	>100 (∼147)

the connection of further TCs. The validation of few-wire protocols for test purposes is one of the objectives of this TVT.

Each motherboard glued on STEPS demonstrator A is loaded with two external dummy units (i.e. small heaters, not connected to the Smart Skin circuits, receiving power directly from outside the TVC, and representing small independent dissipative units). These dummy units are employed to cause symmetric, and asymmetric thermal loads on each motherboard (and on the panel as a whole), and therefore test the ability of the Smart Skin to ensure thermal control under various load conditions.

Dummy units on SDA are represented by small traits of tape heater, with characteristics as per Table 3.30. They are divided in four groups, which can be activated independently. Units in a same group use a parallel connection.

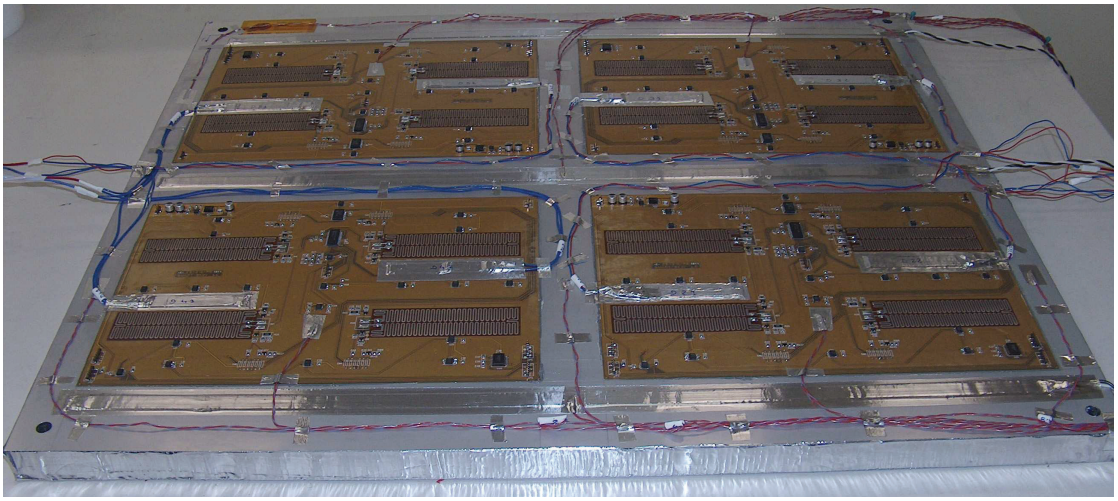

Figure 3.46: Upper face of the SDA panel (+z skin) without MLI.

The SDB cylindrical shell hosts two additional heaters, labeled as H4 and H5 in Figure 3.48. Heater layout and nominal power are shown in Table 3.31. The 2

Table 3.30: Characteristics of dummy units aboard SDA.

Heater #	**Type**	**Length (mm)**	**Resistance (Ω)**	**Max power (W)**
D21	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.88)	> 10 (∼18)
D22	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 ()	> 10 (∼18)
D31	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.61)	> 10 (∼18)
D32	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.73)	> 10 (∼18)
D41	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.57)	> 10 (∼18)
D42	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 ()	> 10 (∼18)
D51	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.60)	> 10 (∼18)
D52	Clayborn (A28, 4 wires, 70 W/ft)	∼ 80	∼1.5 (1.74)	> 10 (∼18)

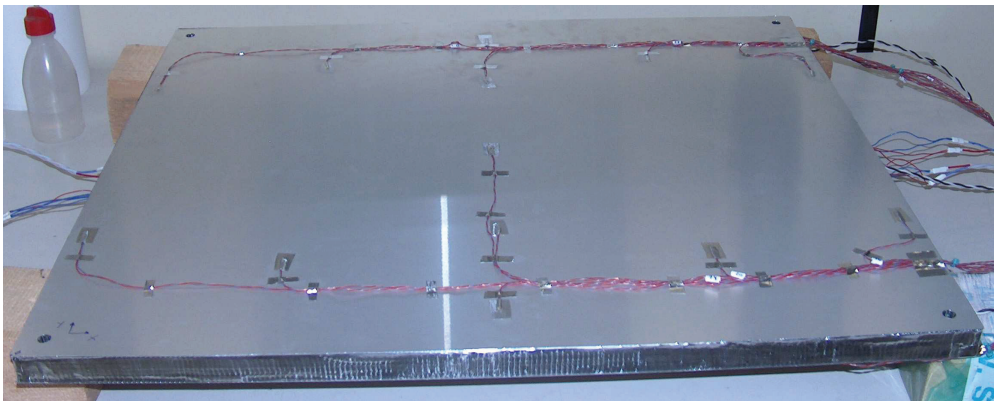

Figure 3.47: Lower face of the SDA panel (-z skin).

Table 3.31: Characteristics of heaters and dummy units aboard SDB.

Heater	Type	Length (mm)	Resistance (Ω)	Max power (W)
H4	Clayborn (A28, 4 wires, 70 W/ft)	~ 220	~5	>50 (50.5)
H5	Clayborn (A28, 4 wires, 70 W/ft)	~ 220	~5	>50 (50.5)
D11	Clayborn (A28, 4 wires, 70 W/ft)	~ 80	~1.5	>10 (~18)
D12	Clayborn (A28, 4 wires, 70 W/ft)	~ 80	~1.5	> 10 (~18)

heaters, in parallel connection, can be activated all together, and in combination with dummy units on the four motherboards.

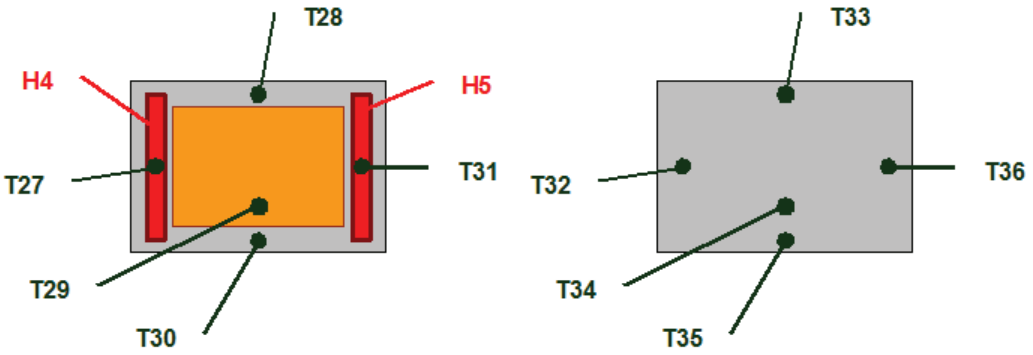

Figure 3.48: Heaters and thermocouples aboard SDB.

The test article is instrumented with a suitable number of temperature sensors (thermocouples):

- 2 TCs on the external side (i.e. facing the chamber) of the MLI blanket and 2 on the internal side.
- 5 TCs on the demonstrator +z skin (electronic side).
- 5 TCs on the demonstrator -z skin (chamber side).

Figure 3.48 shows position and numbering of the 10 SDB thermocouples. Like SDA, this demonstrator hosts a sensor sub-network, too. It is made of 17 direct-to-

digital temperature sensors and is connected with the 4 sub-networks of SDA on the same CAN bus.

Concerning dummy units, STEPS Demonstrator B is equipped with two small tape heater segments as per Table 3.31. They are connected to two different power supplies so that they can be piloted independently (however, to reduce the required overall number of power supplies, each of them can be mounted in parallel with some other units belonging to SDA).

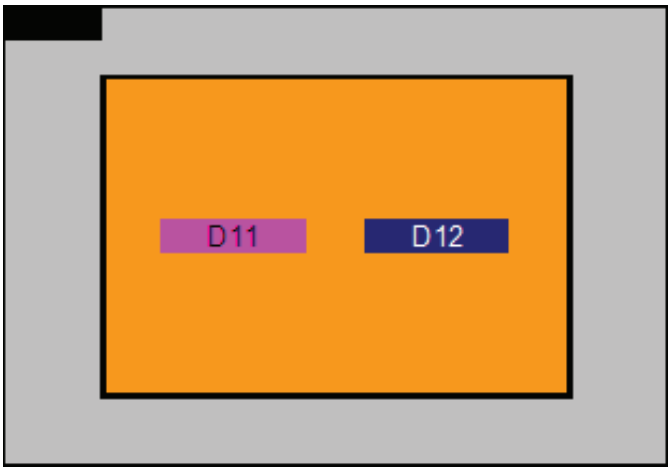

Figure 3.49: Dummy units onboard SDB.

For both panels, where possible, bundles are insulated with 20 layers MLI and properly instrumented with TCs.

The electrical connections are led out of the thermal-vacuum chamber through use of special leakproof feedthroughs.

Additional equipment needed to carry out the test is:

- 2 DC power units (maximum power 1000W), in order to feed the auxiliary heaters aboard the demonstrators.
- 4 DC power units (maximum power ∼200W), in order to feed the dummy units.
- 1 DC power units (maximum power ∼200W), in order to feed the motherboards.
- CAN-USB interface required in order to read CAN data.
- 1 PC, in order to gather and show data from MBs.

The connection of motherboards to the CAN network and to power supply is performed by means of dedicated cables built by NEOHM. These cables are useful connectors that avoid direct soldering of Smart Skin, and allow for an easy set-up of the test article.

In order to understand subsequent diagrams, refer to Figure 3.52 that shows how the smart skin has been schematized. Aboard SDA and SDB, the layout of the motherboards is the one depicted in Figure 3.53 (as seen from the top of the TVC). The connection of all 5 smart skins requires the cables listed in Table 3.32).

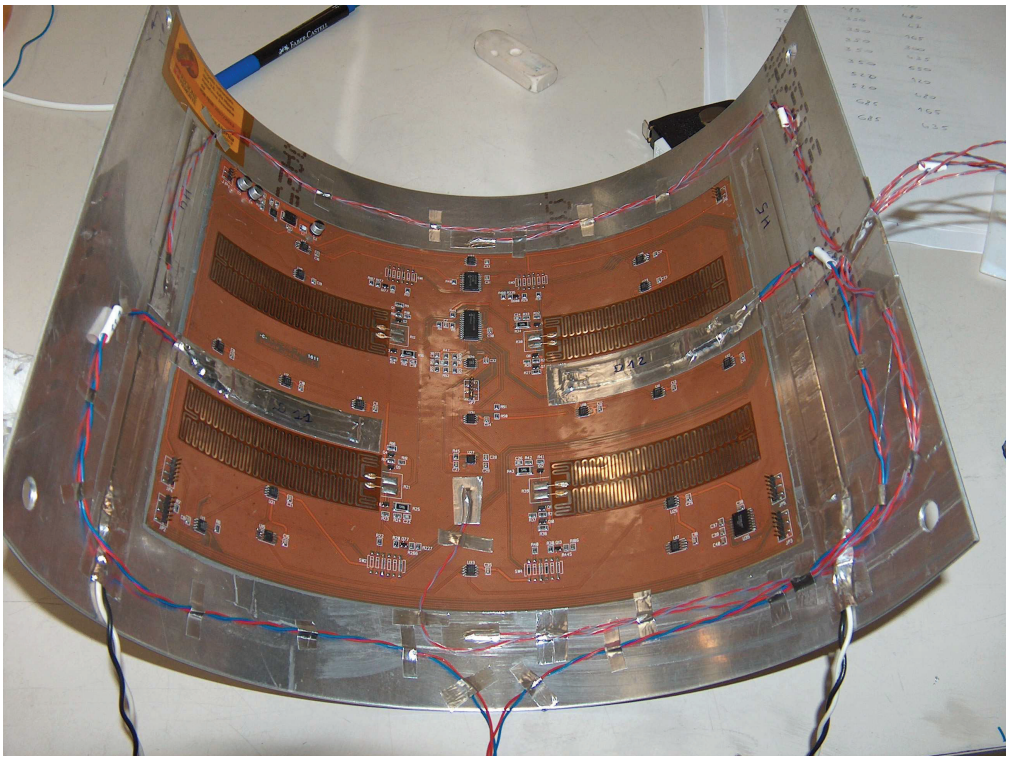

Figure 3.50: Upper face of the SDB panel (+z skin) without MLI.

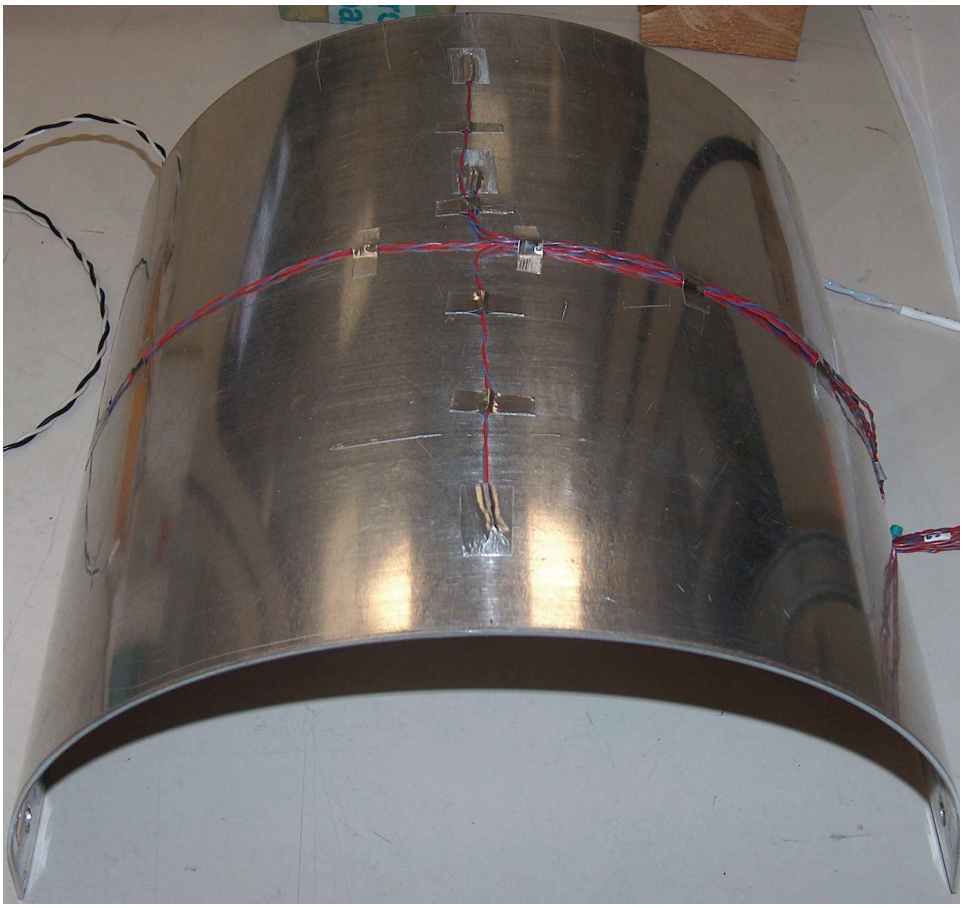

Figure 3.51: Lower face of the SDB panel (-z skin).

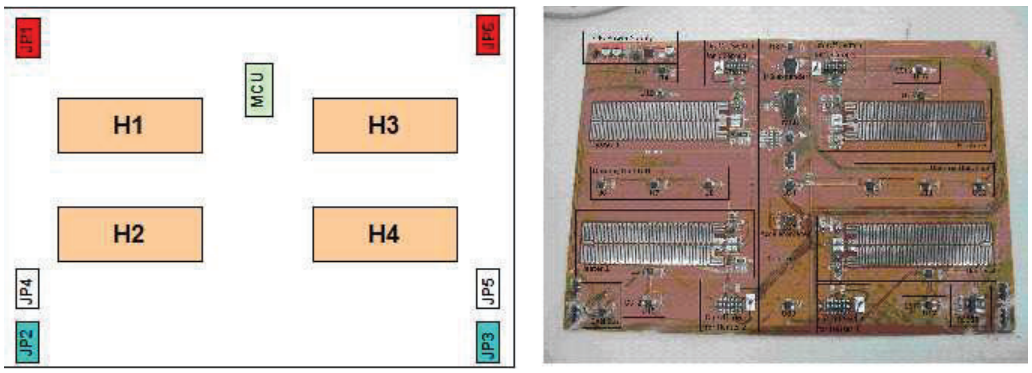

Figure 3.52: Color coding and nomenclature: motherboard schematic compared with smart skin photo.

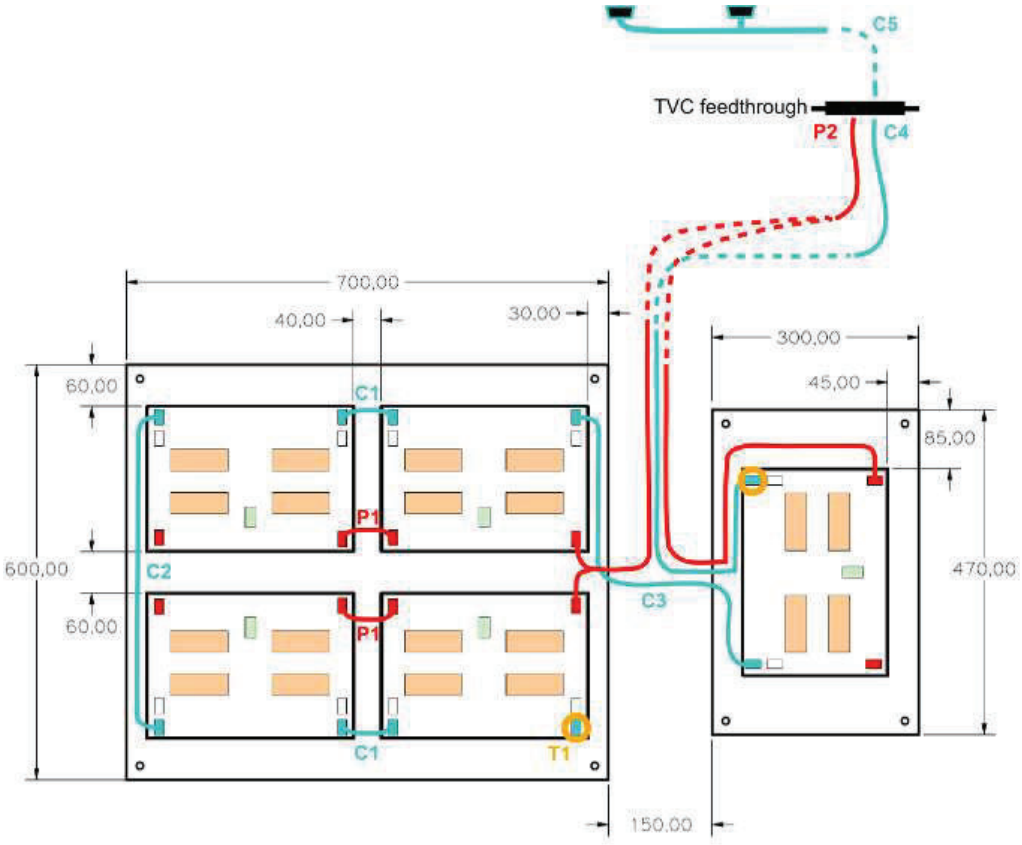

Figure 3.53: Smart skin cabling during TVT (for ease of comprehension, on the right SDB is seen as "deployed"). P2 can be replaced with two separate cables.

Table 3.32: Description of cables required for the TVT.

Quantity	Name	Description	Length	Ref.
2	Power bridge	Simple cable with two sockets. Connects two power ports, crossing a 40 mm gap	∼60 mm	P1
1	Power feed	Cable with three sockets and stripped (bare) wires. Connects (in parallel) three motherboards to the TVC feedthrough. On one end it has bare wires for soldering on feedthrough pins. After 500 mm it has a first split: one cable ends with a female socket and goes directly to SDB; the other cable goes to SDA and, 50 mm before ending is split in two (both terminals host a socket). As an alternative, two separate cables can be separately manufactures and will be soldered together inside the TVC. One cable ends with a female socket and feeds SDB; the other cable goes to SDA and before ending is split in two (both terminals host a socket).	∼3500 mm	P2
2	CAN bridge v1	Simple cable with two sockets. Connects two CAN ports, crossing a 40 mm gap	∼60 mm	C1
1	CAN bridge v2	Simple cable with two sockets. Connects two CAN ports, crossing a 500 mm gap. Can accommodate torsion at both terminals.	∼550 mm	C2
1	CAN bridge v3	Simple cable with two sockets. Connects two CAN ports, crossing a 700 mm gap. Can accommodate torsion at both terminals.	∼800 mm	C3

Table 3.32: Description of cables required for the TVT.

Quantity	Name	Description	Length	Ref.
1	CAN input	Cable with one socket and stripped wires. The socket fits on a CAN port and inserts a 120 Ohm resistor between CAN L and CAN H lines. Bare wires are soldered to the feedthrough pins.	∼3500 mm	C4
1	CAN output	Cable with two DE-9 female connectors (in parallel) and bare stripped wires. Bare wires are soldered on the outer side of TVC feedthrough. The two D-sub 9-pin connectors are needed for CANalyzer and control station.	∼3500 mm	C5
1	CAN terminal	Terminal (single socket) to be mounted at one end of CAN network. It shall be applied to a CAN port and adds a 120 Ohm resistor between CAN L and CAN H lines.	n.a.	T1

Thermal vacuum test approach

The test articles are suspended inside the Leybold vacuum chamber (Figure 3.54). The test consists of a thermal balance test under simulated space environment conditions by thermally controlled shrouds. Test environment conditions are:

- Vacuum: $P < 10e - 5$ bar.
- Shroud temperature: $T = -180$ °C.
- Upper face (+z skin) of the panels (mounting electronics) isolated with 20-layers MLI blanket.
- Lower face (-z skin) exposed to shrouds.

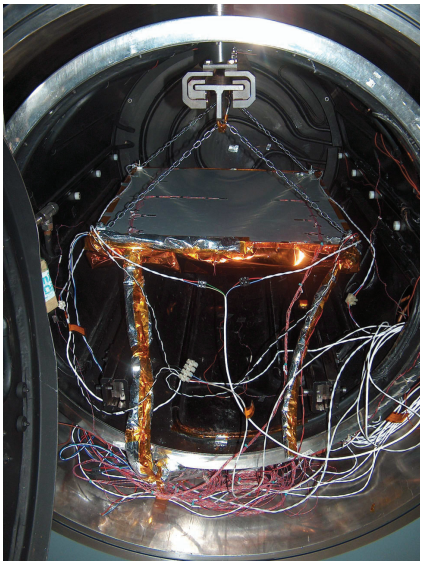

Figure 3.54: Test panel assembly while suspended into the thermal-vacuum test chamber.

Temperature data from the integrated electronics and from auxiliary sensors are acquired for the whole duration of the test with a suitable scan rate (minor or equal to $\Delta t = 60\ s$ for thermocouples, $\Delta t = 5\ s$ for digital sensors).

During three days of test activities, various plateaus are carried out, characterized by different power levels, according to the test sequence described in Table 3.33.

During test, scrupulous attention is paid to COTS electronics requirements, in particular, to limit temperatures. Consult Table 3.34 for details.